AMENDMENT TO THE CLAIMS

Claim 1 (Currently Amended): An apparatus comprising:

an internal oscillating unit for generating an internal multicarrier, said internal oscillating unit comprises:

a constant containing an increase value of each generation carrier;

an accumulator for accumulating constant values of the constant every clock;

a reset for initializing the value when the value of the accumulator exceeds one cycle of sine wave;

a plurality of delays for keeping the values of the accumulator and returning the values to the accumulator in resetting;

a multiplexer and round for multiplexing an output value of the plurality of delays and rounding it off;

a lookup table having a storage of a sine value, for outputting a sine value corresponding to each carrier with an address as the value rounded off by the multiplexer and round; and

a demultiplexer for demultiplexing the sine value and outputting a sine signal of each carrier frequency as an oscillating signal;

a plurality of frequency transition units for respectively down-converting the internal multicarrier generated by the internal oscillating unit and moving it to frequency of "0" as a frequency center; and

a plurality of filtering units for individually filtering a respective carrier moved by the plurality of frequency transition units to the frequency center as the frequency of "0", through a low frequency pass band and for providing the respective carrier as an input to a rake receiver, wherein the apparatus operates to separate carriers of a multicarrier wireless communication receiver system, and operates to separate carriers from a received external multicarrier signal.

Claim 2 (Canceled)

Claim 3 (Currently Amended): The apparatus of ~~claim 2~~claim 1, wherein said reset wraps the address of the lookup table having the storage of the sine signal as the sine wave by using only upper two bits.

Claim 4 (Currently Amended): The apparatus of ~~claim 2~~claim 1, wherein said lookup table requires 4 x 96 having addresses of the 96 number to satisfy an output allowance error of 4 bit, but uses a 4 x 97 lookup table, into which a value equal to a 0^{th} address is entered a 97^{th} address, for the sake of a preparation of the rounding-off.

Claim 5 (Original): The apparatus of claim 1, wherein said internal oscillating unit comprises by a plural number:

constants containing the increase value of each generation carrier;

accumulators for accumulating the constant values of the constant every clock;

resets for initializing the value when the value of the accumulator exceeds a constant value, preferably, one cycle of the sine wave;

delays for keeping the values of the accumulator and returning the values to the accumulator in resetting;

rounds for rounding the output value of the delay off; and

a plurality of lookup tables having the storage of the sine value, for outputting the sine value corresponding to each carrier with the address as the value rounded off by the round.

Claim 6 (Original): The apparatus of claim 5, wherein said reset wraps the address of the lookup table having the storage of the sine signal as the sine wave by using only upper two bits.

Claim 7 (Original): The apparatus of claim 5, wherein said lookup table requires 4 x 96 having addresses of the 96 number to satisfy an output allowance error of 4 bit, but uses a 4 x 97 lookup table, into which a value equal to a 0^{th} address is entered a 97^{th} address, for the sake of a preparation of the rounding-off.

Claim 8 (Original): The apparatus of claim 1, wherein said plurality of frequency transition units use six multipliers and make frequency electricity of each carrier same in order to make the frequency down-adjusting number equal, to thereby control electricity of the carrier easily.

Claim 9 (Original): The apparatus of claim 8, wherein said plurality of filtering units are a 64 tap low frequency band pass filter of a 6bit filter input as an FIR filter for converting 6 bit input as a complement type of 2 into six single bits, processing a low frequency band pass filter (FIR filter) computation of several single bit inputs in one independent filter, and accumulating them in six of bit units, to finally output a filter output value of 6bit input, even without using the multiplier.

Claim 10 (Original): The apparatus of claim 9, wherein said low frequency band pass (FIR) filter comprises:

six 64bit shift registers for making 6bit filter inputs as the complement type of 2, single bit, and shifting and storing them;

a selector for selecting one out of input data stored at six 64bit shift registers;

an address generator for generating the address so as to be matched with the lookup table divided into the eight number by using input data selected in the selector;

a lookup table divided into the eight number with the address generated in the address generator, each lookup table being reduced in a size thereof by using a symmetry provided within the lookup table;

a computing part for computing outputs of eight lookup tables by a most significant bit (MSB) control of each lookup table address, adding up them, and thereby generating filter outputs corresponding to respective filter input bits; and

an accumulator for right-shifting the filter output per bit and accumulating by the number of coefficients

Claim 11 (Original): The apparatus of claim 10, wherein said address generator is constructed by exclusive logical sum (XOR) gates for performing an exclusive logical sum (XOR) computation by using a most significant bit (MSB) of an inputted address, in order for an access to an address of an omitted lookup table by using a symmetry within the lookup table.

Claims 12-13 (Cancelled)

Claim 14 (New): An apparatus comprising:

an internal oscillating unit for generating an internal multicarrier, said internal oscillating unit comprises by a plural number:

constants containing the increase value of each generation carrier;

accumulators for accumulating the constant values of the constant every clock;

resets for initializing the value when the value of the accumulator exceeds a constant value, preferably, one cycle of the sine wave;

delays for keeping the values of the accumulator and returning the values to the accumulator in resetting;

rounds for rounding the output value of the delay off; and

a plurality of lookup tables having the storage of the sine value, for outputting the sine value corresponding to each carrier with the address as the value rounded off by the round;

a plurality of frequency transition units for respectively down-converting the internal multicarrier generated by the internal oscillating unit and moving it to frequency of "0" as a frequency center; and

a plurality of filtering units for individually filtering a respective carrier moved by the plurality of frequency transition units to the frequency center as the frequency of "0", through a low frequency pass band and for providing the respective carrier as an input to a rake receiver,

wherein the apparatus operates to separate carriers of a multicarrier wireless communication receiver system, and operates to separate carriers from a received external multicarrier signal.

Claim 15 (New): The apparatus of claim 14, wherein said reset wraps the address of the lookup table having the storage of the sine signal as the sine wave by using only upper two bits.

Claim 16 (New): The apparatus of claim 14, wherein said lookup table requires 4 x 96 having addresses of the 96 number to satisfy an output allowance error of 4 bit, but uses a 4 x 97 lookup table, into which a value equal to a 0^{th} address is entered a 97^{th} address, for the sake of a preparation of the rounding-off.